REMARKS

This is in response to the Office Action dated July 25, 2002. In view of the foregoing amendments and following representations, reconsideration is respectfully requested.

Initially, on page 2 of the Office Action, the Examiner responds to the traversal of the restriction requirement. The Examiner maintains the requirement based on the contention that "the claims in the present application are not identical in scope to the claim in the parent application." The Examiner is requested to reconsider the requirement because the claims, which were withdrawn by the Examiner, are identical to claims that were considered in the parent application. Therefore, for the reasons set forth in the paper filed on March 15, 2002, the Examiner is requested to withdraw the restriction requirement, and examine claims 37-47 along with claims 26-36.

* * * * *

Next, on pages 2-3 of the Office Action, claims 26-36 are rejected as follows:

Claims 26-32, 34 and 36 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hashimoto (USPN 6,201,193); and

Claims 26 and 33-36 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hertz et al. (USPN 5,381,307).

It is submitted that the present invention, as embodied by claims 26-36, distinguishes over the applied prior art references for the following reasons.

The present invention, as defined in claim 26, is directed an electronic component having a reference mark, which is **located on a surface of the component** and serves as a reference of the arrangement positions of the electrical connecting portions. For the Examiner's convenience, a sketch, which includes the claimed arrangement, is attached.

Note that the claimed surface of the component is a surface that confronts the board as shown in Figs. 3A and 3B, or another surface of the component that is opposite relative to the confronting surface as shown in Figs. 6A and 6B.

Therefore, with the claimed invention it is not necessary to provide a mark on the board, and thus, any type of board can be used in the disclosed mounting process.

In contrast, **Hashimoto** discloses that marks 25 and 36 are **formed on a circuit board** (see Fig. 9). In particular, lines 31-33 of column 12 of Hashimoto state:

> "As shown in FIG. 9, on the printed circuit board 2 of the present invention are also provided four marks 25 for positioning the TCP when the TCP is mounted." (emphasis added)

Furthermore, in describing the mounting process, the Hashimoto reference indicates that:

> "The positioning marks 25 are recognized at a stage before the step of setting the TCP 3 on the circuit board 2. Therefore, there is no problem even if the marks are provided in the area where the CPU is fixed as in the case of the present invention.
>
> Conventionally, such positioning marks are ordinarily provided in an area outside the lands 8, as indicated by ghost-image marks 26 as shown in FIG. 9. Even in a case where such positioning marks are provided inside the lands 8, they are disposed at arbitrary positions on the printed circuit board even in a signal conductor wiring area." (column 12, lines 57-67)

Also, as described in column 13, lines 24-31 of Hashimoto, marks 30 are **formed on a circuit board**.

Therefore, each of the marks disclosed in Hashimoto are formed on a circuit board. This is similar to the "prior art" arrangement illustrated in Fig. 15 of the present application, in which the marks 3 are formed on the circuit board. As discussed above, claim 26

specifies that the mark is provided on **a surface of the component**. Clearly the arrangement defined in claim 26 is not disclosed or suggested by Hashimoto.

Hertz discloses that marks 504 that are formed on a circuit board. More specifically, the Hertz reference describes that:

> "FIG. 5 is a top view of the surface area 402 of the circuit supporting substrate 202 ..... . By dimensioning and arranging the aligning pads 504 relative to their corresponding leads 406 it assures that at one of the aligning pads 506, 510, 514, 518, will at least partially overlap with its paired lead 508, 512, 516, 520, on the component." (col. 6, lines 18-44)

Note that the other marks 506, 510, 514, 518 disclosed in Hertz, are also formed on the circuit board. Therefore, the marks disclosed in the Hertz reference are merely formed on a circuit board. As with Hashimoto, the marks disclosed in Hertz as similar to the "prior art" marks 3 shown in Fig. 15 of the present application. Therefore, Hertz does not disclose or suggest an arrangement in which the marks are formed on **a surface of the component**.

As demonstrated above, the collective teachings of the Hashimoto and Hertz references do not disclose or suggest each and every limitation of claim 26, which requires, *inter alia*, an electronic component having at least one reference mark provided on a surface of the component. Therefore, claims 26-36 are allowable over the prior art of record.

In view of the above, it is submitted that the present application is now clearly in condition for allowance. The Examiner therefore is requested to pass this case to issue.

In the event that the Examiner has any comments or suggestions of a nature necessary to place this case in condition for allowance, then the Examiner is requested to

contact Applicant's undersigned attorney by telephone to promptly resolve any remaining matters.

Respectfully submitted,

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Version with Markings to
Show Changes Made

IN THE CLAIMS:

Please amend claims 26, 29 and 33 as follows (*a clean set of all pending claims is presented for the Examiner's convenience):*

26.(AMENDED) An electronic component to be mounted on a printed board, said electronic component comprising:

an electrical connecting surface;

a plurality of electrical connecting portions provided on said electrical connecting surface in arrangement positions; and

at least one reference mark located on a surface of the electronic component and serving [that serves] as a reference for the arrangement positions of said electrical connecting portions.

27. An electronic component as claimed in claim 26, wherein said at least one reference mark comprises a pair of reference marks positioned symmetrically with respect to a center point of said electrical connecting surface, wherein said electrical connecting portions are disposed in an array that surrounds said reference marks.

28. An electronic component as claimed in claim 26, wherein said at least one reference mark comprises a plurality of reference marks that are positioned symmetrically with respect to a center point of said electrical connecting surface, wherein said reference marks are located in a central portion of said electrical connecting surface, and said electrical connecting portions are disposed around said reference marks.

29.(Amended) An electronic component as claimed in claim 26, wherein said reference mark is provided on a side of said electrical connecting surface that is adapted to [faces] confront a mounting position of the printed board.

30. An electronic component as claimed in claim 29, wherein said reference mark comprises a projection or a printed symbol.

31. An electronic component as claimed in claim 29, wherein said reference mark includes coded information indicative of said electronic component.

32. An electronic component as claimed in claim 31, wherein the coded information of said reference mark is information concerned with a state in which the electrical connecting portions are formed.

33.(amended) An electronic component as claimed in claim 26, wherein said reference mark is located in a corner portion of an opposite side of the electronic component relative to said electrical connecting portions [said electrical connecting surface].

34. An electronic component as claimed in claim 26, wherein said reference mark is formed on said electrical connecting surface simultaneously with said electrical connecting portions.

35. An electronic component as claimed in claim 26, wherein said electrical connecting portions are solder bumps.

36. An electronic component as claimed in claim 26, wherein said electrical connecting portions are lands.